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VLSI Testing 2006 Spring Instructor: Jin-Fu Li. Email: jfli@cc.ncu.edu.tw Homeworks Homework 1-March 20- Homework 2-April 6- Material Chapter 0. VLSI Testing Syllabus Chapter 1. Introduction Chapter 2. Fault Modeling Chapter 3. Testability Measures Chapter 4. Fault Simulation Chapter 5. Combination and Sequential. Circuit Test Generation Chapter 6

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Advanced Reliable Systems (ARES) Lab. Jin-Fu Li, EE, NCU 28 1. Set test input to all test points 2.Apply the master reset signal to initialize all memory elements 3.Set scan-in address and data, and then apply the scan clock 4.Repeat step 3 until all internal test inputs are scanned in 5.Clock once for normal operation 6.Check states of the ...

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VLSI TEST AUTOMATION TEST ALGORITHMS & GENERATION 6-1 6 TEST ALGORITHMS & GENERATION In what follows, we discuss some of the test used in generating tests, including Boolean difference, D-Algorithm, and Critical Path. These types of algorithms are used to generate test patterns.

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